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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,905	06/26/2001	Gwan-Byeob Koh	5649-873	1424

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MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER
GEBREMARIAM, SAMUEL A

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/891,905	Applicant(s) KOH ET AL.
	Examiner Samuel A Gebremariam	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 17-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 17-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1, 2, 3, 17, 21, 22, 23 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Odake US patent No. 6,165,825.

Regarding claims 1, 21 and 24, Odake teaches (figs. 5a-5f) a method of forming a channel region (10, 18) between isolation regions (2) of an integrated circuit substrate (1), the method comprising: forming a mask (Pr21) on the isolation region that extends onto a portion of the substrate adjacent to the isolation region to provide a shielded portion of the substrate adjacent to the isolation region (see fig. 5a) and an exposed portion of the substrate spaced apart from the isolation region having the shielded portion therebetween, the exposed portion of the substrate comprising a first portion where a gate electrode (region above 10 and 18) will be subsequently formed and a second portion where a bit line contact will be subsequently formed, the mask exposing only the first and second portions; implanting ions (refer to fig. 5a) into the exposed portion of the substrate using the mask as an implant mask, thereby forming a channel region in only the first and second portions to adjust the threshold voltage of a transistor (10); forming a plurality of gate electrodes (fig. 5f) on the channel region; and implanting

ions using the plurality of gate electrodes as an implant mask to form source/drain regions associated with the plurality of gate electrodes and to define separate channel regions from the channel region that are self-aligned to the plurality of gate electrodes (col. 12, line 60- col.13, line 12).

The formation of gate electrode structures in the region Rn1 and Rp1 and the ion implantation performed using the gate structures as implantation mask inherently defines a channel region that is different from the one formed before the gate structures are formed. Furthermore Odake forms more than one gate electrode as illustrated in figure 5f where regions Rn1 and Rp1 are shown. Therefore Odake teaches a plurality of gate electrodes.

Regarding claims 2 and 22, Odake teaches the entire claimed process of claim 1 above including forming the channel region comprises; implanting a first level of ions in the shielded region adjacent to the isolation region and implanting a second level of ions in the channel region spaced apart from the isolation region where the second level is greater than the first level (figs. 5a-5f and column 11, lines 52-64).

Regarding claims 3 and 23, Odake teaches substantially the entire claimed process of claim 1 above including implanting boron ions in the exposed region in order to form a single channel region (10).

Regarding claim 17, Odake teaches the entire claimed process of claim 1 above including at least one of the source/drain regions is in the exposed portion (fig. 5f).

Regarding claim 18, Odake teaches (fig. 5c) the entire claimed process of claim 1 above including implanting first ions of first conductive type and implanting second ions of second conductive type (col. 12, line 8-14).

Regarding claim 20, Odake teaches (fig. 5f) the entire claimed process of claim 1 above including the source/drain regions comprise lightly doped source/drain (15,17) structures.

Regarding claim 21, Nara teaches a method of forming a channel region between isolation regions of an integrated circuit substrate, the method comprising: forming a mask (5) on first and second adjacent isolation regions (2) in an integrated circuit substrate (1) and extending onto an active area between the first and second isolation regions to define first and second shielded portions (fig. B) adjacent to the first and second isolation regions and an exposed portion of the substrate; forming a single channel region (6) (fig. C) in the exposed portion of the substrate; forming a plurality of gate electrodes (4) on the single channel region and implanting ions using a plurality of the gate electrodes as an implant mask to form source/drain regions (7) associated with the plurality of the gate electrodes and to form first and second spaced apart channel regions from the single channel region (6) (figs. A-E).

Regarding claim 22, Nara teaches the entire claimed process of claim 1 above including implanting ions comprises implanting ions to form the first and second spaced apart channel regions self-aligned to the plurality of the gate electrodes (figs. C-D).

Regarding claim 23, Nara teaches the entire claimed process of claim 1 above including forming a single channel region (6) comprises implanting boron ions in the exposed portion (page 2, translation drawing C).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 19, is rejected under 35 U.S.C. 103(a) as being unpatentable over Nara.

Odake teaches substantially the entire claimed process of claim 1 above except explicitly stating that the implant step of claim 18 comprises implanting boron ions to provide a first concentration of about $1x10^{17}$ ions/cm^3.

Parameters such as dopant concentration and dopant type in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during device fabrication.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the boron concentration as claimed in order to improve the threshold voltage of the device.

Response to Arguments

3. Applicant's arguments with respect to claims 1-3, and 17-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on 8:00am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 305-7646. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
February 23, 2003

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800